#### Weak memory models using event structures

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March 25, 2016 Gallium Seminar A simple concurrent and imperative program:

$$\begin{array}{c|c} x, y \text{ initialized to } 0\\ x := 1 & y := 2\\ r \leftarrow y & s \leftarrow x\\ \text{shared variable} \cdot \text{local register} \end{array}$$

Expected outcome:  $r \neq 0 \lor s \neq 0$ .

A simple concurrent and imperative program:

$$\begin{array}{c|c} x, y \text{ initialized to } 0 \\ r \leftarrow y \\ x := 1 \end{array} \begin{vmatrix} s \leftarrow x \\ y := 2 \end{vmatrix}$$
shared variable  $\cdot$  local register

Expected outcome:  $r \neq 0 \lor s \neq 0$ . Wrong on modern architectures (x86, ARM, ...).

### Unexpected behaviours

Another simple program:

$$\begin{array}{c|c} x := 1 \\ r_1 \leftarrow x \\ r_2 \leftarrow y \end{array} \begin{vmatrix} y := 1 \\ s_1 \leftarrow y \\ s_2 \leftarrow x \end{vmatrix}$$

Expected outcome:  $r_1 = s_1 = 1 \Rightarrow r_2 = s_2 = 1$ 

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Expected outcome:  $r_1 = s_1 = 1 \Rightarrow r_2 = s_2 = 1$ 

Wrong even without read exchange (Read Own Write Early).

## A need to specify the behaviour

What are the expected behaviour of a concurrent programs?  $\rightarrow$  It depends on the architectures.

Architectures need to be specified:

- what instructions can be reordered?
- how are writes propagated from one thread to the other?

## A need to specify the behaviour

What are the expected behaviour of a concurrent programs?  $\rightarrow$  It depends on the architectures.

Architectures need to be specified:

- what instructions can be reordered?
- how are writes propagated from one thread to the other?

To that end, manufacturers provide prosaic documents, but:

- ambiguity: behaviours that are not specified
- inconsistent: some observations may not be predicted.

Some architectures:

- ▶ SC (Sequential consistency): no reordering, sequential memory,
- ARM: reordering of instructions targeting different variables, write caches.

▶ x86: ...

#### Semantics saves the day

Semantics: Formalize mathematically the vendors specifications:

- get a (possibly computer-verified) proof of non-ambiguity,
- implement the specifications and mechanically test it against real life architectures.

Two main types of semantics among existing models:

- operational semantics: executions are described by the runs of an abstract machines,
- axiomatic semantics: the notion of valid execution is axiomatized.

Those models are called *weak memory models*.

## Semantics and executions

The semantics generates from a program its possible executions:

ProgramSome executions
$$x := 1 \parallel y := 2$$
 $\mathbb{W}_{x}^{(1)} \cdot \mathbb{W}_{y}^{(2)} \cdot \mathbb{R}_{y}^{(2)} \cdot \mathbb{R}_{x}^{(1)}$  $r \leftarrow y \parallel s \leftarrow x$  $\mathbb{W}_{y}^{(2)} \cdot \mathbb{R}_{x}^{(0)} \cdot \mathbb{W}_{x}^{(2)} \cdot \mathbb{R}_{y}^{(1)}$ 

*Executions* can be formalized in different ways: traces, partial-order, ...

# This talk

A semantics that is

- denotational: executions computed by induction
  - the semantics is thus compositional
- compact: based on event structures
  - no combinatorial explosion
- extensible: inspired from game semantics
  - ▶ it is easy to add loops, control operators, higher-order, ...

Outline of the talk:

- 1. A semantics warm-up: compute the SC semantics using *traces*.
- 2. Getting back the **causality**.
- 3. Our contribution: A **parametric** semantics using event structures.
- 4. A game semantics aparté at the end (if time allows)

#### I. A denotational semantics for SC

With traces of originality

#### Syntax precedes semantics

Our very simple programming language:

$$e, e' ::= \{ Expressions \} \\ k \in \mathbb{N} \mid r \in \mathcal{R} \mid e + e' \\ \iota ::= \{ Instructions \} \\ \mid a := e \qquad (Write on a variable) \\ \mid r \leftarrow a \qquad (Read on a variable) \\ t ::= \{ Threads \} \\ \mid \iota; \dots; \iota \\ p ::= \{ Programs \} \\ t_1 \parallel \dots \parallel t_n \end{cases}$$

In real life: conditionals and barriers.

#### Denotational semantics

**Goal**: compute  $\llbracket t \rrbracket \in E$  where *E* is some space of denotations.

Our space here: langages of traces.

$$\begin{split} \Sigma_{a} &= \mathcal{V} \times \{\mathtt{R}, \mathtt{W}\} & (\text{Abstract memory event})\\ \Sigma_{c} &= \Sigma_{a} \times \mathbb{N} & (\text{Concrete memory event})\\ E &= \mathscr{P}(\Sigma_{c}^{*}) \end{split}$$

Notations:  $\mathbf{R}_{X}^{(k)}$ ,  $\mathbf{W}_{X}^{(k)}$ .

Two steps:

- Volatile semantics [[t]]<sup>O</sup>: shared variables are considered volatile: [[x := 1; r ← x]]<sup>O</sup> does not guarantee to read 1 in r.
- Closed semantics: once [[t]]<sup>O</sup> is calculated for the whole program, we restrict the scope of the variable [[x := 1; r ← x]] reads 1 in r.

### Volatile semantics

**Semantics of threads.** Parametrized over  $\rho : \mathcal{R} \to \mathbb{N}$ .

(Writes) 
$$\llbracket x := e; t \rrbracket \rho = \mathbb{W}_{\times}^{(\rho(e))} \cdot \llbracket t \rrbracket \rho$$
  
(Reads)  $\llbracket r \leftarrow x; t \rrbracket \rho = \bigcup_{i \in \mathbb{N}} \left( \mathbb{R}_{\times}^{(i)} \cdot \llbracket t \rrbracket (\rho[r \leftarrow i]) \right)$ 

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**Semantics of programs.** Obtained by interleaving  $(\circledast)$ :

$$\llbracket t_1 \parallel \ldots \parallel t_n \rrbracket = \llbracket t_1 \rrbracket \emptyset \circledast \ldots \circledast \llbracket t_n \rrbracket \emptyset$$

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**Example.** Define 
$$p = (x := 1; y \leftarrow r \parallel y := 1; x \leftarrow s)$$
  
 $\mathbb{W}_{x}^{(1)} \cdot \mathbb{W}_{y}^{(1)} \cdot \mathbb{R}_{y}^{(3)} \cdot \mathbb{R}_{x}^{(2)} \in \llbracket p \rrbracket$   
 $\mathbb{W} \operatorname{R}_{x}^{(0)} \cdot \mathbb{R}_{y}^{(0)} \cdot \mathbb{W}_{x}^{(1)} \cdot \mathbb{W}_{y}^{(1)} \notin \llbracket p \rrbracket.$ 

#### Closed semantics

Obtained by eliminating "inconsistent" traces (eg.  $W_{X}^{(2)} \cdot R_{X}^{(3)}$ )

Linear memory model. A language of "consistent" traces:

$$egin{aligned} \mathcal{M}(\mu:\mathcal{V} o\mathbb{N}) &::=\epsilon \ &\mid \mathtt{R}^{(\mu( imes))}_{ imes}\cdot\mathcal{M}(\mu) \ &\mid \mathtt{W}^{(k)}_{ imes}\cdot\mathcal{M}(\mu[ imes\leftarrow k]) \ &\mathcal{M}::=\mathcal{M}( imes\leftarrow 0) \end{aligned}$$

Closed semantics:  $\llbracket p \rrbracket = \llbracket p \rrbracket^O \cap M$ .

**Example.** Write  $p = (x := 1; r \leftarrow y) \parallel (y := 2; s \leftarrow x)$ • every trace of  $\llbracket p \rrbracket$  ends with  $R_x^{(1)}$  or a  $R_y^{(2)}$ .

## Summary

#### Advantages.

- Easy to define semantics, by induction on programs.
- By making *M* more complex, complex cache schemes can be handled

#### Drawbacks.

- Combinatorial explosion due to interleavings.
- How to model reordering of instructions?

#### Towards partial-orders.

- Because of reorderings, threads are not totally ordered
- Our goal: compute fine precisely dependencies between the instructions, given an architecture.

#### II. Event structures

#### Raiders of the lost causality

Idea: volatile semantics should be a set of partial-orders.

Term:

$$x := 1; y := 1;$$
  

$$r \leftarrow x; s \leftarrow y;$$
  

$$z := s + t$$

Idea: volatile semantics should be a set of partial-orders.

Dependencies (depends on the architecture):

Idea: volatile semantics should be a set of partial-orders.

Executions (depends on the architecture):



- traces on Σ<sub>c</sub> becomes *partially ordered multisets* over Σ<sub>c</sub> (pomsets)
- $\llbracket t \rrbracket^O$  becomes a set of such *pomsets*.

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Executions (depends on the architecture):



- traces on Σ<sub>c</sub> becomes partially ordered multisets over Σ<sub>c</sub> (pomsets)
- $[t]^O$  becomes a set of such *pomsets*.
- Problem: lots of redundancies in the pomsets..

## Can we sum up all executions in a single object?

Can we glue the executions all together in a partial-order? For instance:



Which sets of events w are (partial) executions?

• w must be downward-closed for  $\rightarrow$ 

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Which sets of events w are (partial) executions?

- w must be downward-closed for  $\rightarrow$
- ▶ and ...?  $\{W_x^{(1)}, R_x^{(0)}, R_x^{(1)}\}$  cannot be a valid execution.

#### $\Rightarrow$ Need more structure than a partial-order: conflicts.

#### Definition (Event structures)

A set of event E with:

- A notion of **causality** represented by a partial order  $\leq_E$
- A notion of **conflict** represented by a relation  $\sim_E$
- A labelling  $I : E \to \Sigma$ .

(+ axioms)

Definition (Configuration or partial execution) A configuration of E is a subset w of E:

- downward-closed:  $e \leq e' \in w \Rightarrow e \in w$ .
- that does not contain two conflicting events

On the example:



On the example:



We have the configuration:

 $W_x^{(1)}$ 

On the example:



We have the configuration:

$$\begin{array}{c} \mathbb{W}_{x}^{(1)} \\ \downarrow \\ \mathbb{R}_{x}^{(1)} \end{array}$$

On the example:



We have the configuration:



On the example:



We have the configuration:



On the example:



We have the configuration:



#### III. DESIGNING A SEMANTICS WITH EVENT STRUCTURES

Dessine-moi une structure d'événements

## Defining architectures

Now we define an architecture  $\mathscr{A}$  as a pair  $(\rightarrow_{\mathscr{A}}, E)$ :

- ►  $\rightarrow_{\mathscr{A}} \subseteq \Sigma_a \times \Sigma_a$  indicates which causality cannot be erased.
- $E_{\mathscr{A}}$  is an event structure representing the memory model.

Examples for 
$$\rightarrow_{\mathscr{A}}$$
:  
 $\blacktriangleright \rightarrow_{SC} = \Sigma_a \times \Sigma_a$   
 $\blacktriangleright \rightarrow_{ARM} = \{(e, e') \mid v(e) = v(e')\} (v(x, \_) = x).$   
 $\blacktriangleright \rightarrow_{x86} = ...$ 

Examples for  $E_{\mathscr{A}}$  include all languages  $M \subseteq \Sigma_c^*$  (they can be viewed as event structures).

Computing the semantics  $[\![p]\!]_{\mathscr{A}}$ 

As previously, in two steps:

- Volatile semantics:
  - threads: [[t]]<sup>O</sup><sub>A</sub> is defined as previously but where the causality outside →<sub>A</sub> are relaxed.
  - ▶ programs: [[t<sub>1</sub> || ... || t<sub>n</sub>]]<sup>O</sup><sub>𝒜</sub> = [[t<sub>1</sub>]]<sup>O</sup><sub>𝒜</sub> || ... || [[t<sub>n</sub>]]<sup>O</sup><sub>𝒜</sub> where || is parallel composition.

► Closed semantics: [[p]]<sub>A</sub> = [[p]]<sup>O</sup><sub>A</sub> ∧ E<sub>A</sub> where ∧ is the synchronized product: a generalization of intersection of languages to event structures.








(x86)



#### (ARM)





# The memory model ${\mathscr E}$

Define a consistent execution to be a  $\Sigma_c$ -labelled partial-order  $(q, \leq_q)$  satisfying:

1. Write serialization. Writes on a variable are totally ordered.

$$egin{array}{ccc} \mathbb{W}^{(1)}_{\scriptscriptstyle{X}} & 
otline & \mathbb{W}^{(3)}_{\scriptscriptstyle{X}} & 
otline & \mathbb{W}^{(4)}_{\scriptscriptstyle{X}} & 
otline & \mathbb{W}^{(2)}_{\scriptscriptstyle{Y}} & 
otline & \mathbb{W}^{(0)}_{\scriptscriptstyle{Y}} & 
otline & \mathbb{W}^{(0)}_{\scriptscriptstyle{Y}$$

2. Coherent reading. For  $e = \mathbb{R}^{(k)}_{\times} \in q$ ,  $\mathbb{W}^{(k)}_{\times}$  is the maximal event of  $\{\mathbb{W}^{(n)}_{\times} \in q \mid \mathbb{W}^{(n)}_{\times} \leq e\}$ 



**Theorem.** There is an event structure  $\mathcal{E}$  whose configurations are exactly consistent partial-orders. Weak memory models using event structures Simon Castellan



(Volatile semantics for SC)



(Computing  $\llbracket p \rrbracket_{SC}^O \land \mathscr{E}$ )



(Computing  $\llbracket p \rrbracket_{SC}^O \land \mathscr{E}$ )

 $p = \begin{array}{c|c} x := 1 \\ r_1 \leftarrow x \\ r_2 \leftarrow y \end{array} \begin{vmatrix} y := 1 \\ s_1 \leftarrow y \\ s_2 \leftarrow x \end{vmatrix}$  $\mathbb{W}_{x}^{(1)}$   $\downarrow$  $W_y^{(1)}$ 

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We can observe  $r_1 = s_1 = 1 \land r_2 = s_2 = 0$ .

## $\ensuremath{\mathcal{E}}$ is too relaxed

Consider 
$$p = \begin{pmatrix} x := 1 \\ s \leftarrow y \\ t \leftarrow x \end{pmatrix}$$
  $\begin{pmatrix} r \leftarrow x \\ t \leftarrow x \end{pmatrix}$ 

The denotation  $\llbracket p \rrbracket_{SC}^O \land \mathscr{E}$  contains the configuration:

$$egin{array}{cccc} \mathbb{W}^{(1)}_{ imes} & \Rightarrow \mathbb{R}^{(1)}_{ imes} & \mathbb{W}^{(1)}_{ imes} & & \mathbb{W}^{(1)}_{ imes} \ & & \downarrow & & \ & & \downarrow & & \ & & \mathbb{R}^{(0)}_{ imes} & \mathbb{R}^{(0)}_{ imes} & \mathbb{R}^{(0)}_{ imes} \end{array}$$

This allows the observation:  $r = 1 \land s = t = 0$  which is not possible with TSO (x86's memory model).

**Problem.** With TSO, writes becomes visible to *all others* threads at the same time.

# Defining &TSO

1. We need our model to be "thread-aware":

$$\begin{array}{ccc} \mathbb{W}^{(1,1)}_{\times} \to \mathbb{R}^{(2,1)}_{\times} & \mathbb{W}^{(3,1)}_{\times} \\ \downarrow & \downarrow \\ \mathbb{R}^{(2,0)}_{\times} & \mathbb{R}^{(3,0)}_{\times} \end{array}$$

2. Say a consistent execution satisfies the TSO criterion, when:

for all writes  $w \in q$ , for all *incomparable* reads  $r, r' \in q$  in a different thread than w $(w \leq r)$  iff  $(w \leq r')$ 

3. Define  $\mathscr{E}_{TSO}$  to be the set of consistent execution satisfying this criterion.

#### IV. THE GAME SEMANTICS BEHIND ALL THAT

La sémantique des jeux vue du ciel

# Idealized Parallel Algol

A

Throwing in simply-typed  $\lambda$ -calculus to our language we get **IPA**:

$$\begin{array}{l} A,B := \operatorname{int} |\operatorname{var}| \operatorname{unit} | A \Rightarrow B \\ t,u := x | \lambda x. t | t u \\ | \operatorname{read}^{\operatorname{var} \to \operatorname{unit}} | \operatorname{write}^{\operatorname{var} \to \operatorname{int} \to \operatorname{unit}} \\ | \operatorname{new} x^{\operatorname{var}} \operatorname{in} t \quad (t \text{ has type int or unit}) \\ | (t; u) | (t \parallel u) \end{array}$$

- Comes with an SC and call-by-name operational semantics.
- Giving semantics: a semantics for λ-calculus plus operators for read, write, ...
- Games semantics: types  $\rightarrow$  games, programs  $\rightarrow$  strategies.
- ► We have good trace-based games model for that.

An example.

 $x: \texttt{var} \to \texttt{int}$ 

Problem. No access to the continuation to break causalities.

An example.

 $x: \texttt{var} \to \texttt{int}$ 

ask

Problem. No access to the continuation to break causalities.

An example.



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Problem. No access to the continuation to break causalities.

The read operation becomes let : var  $\rightarrow$  (int  $\rightarrow$  unit)  $\rightarrow$  unit:

let read x f =  
let 
$$z = !x$$
 in f z

$$x: \texttt{var} 
ightarrow f: (\texttt{int} 
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ightarrow \texttt{unit}$$

The read operation becomes let : var  $\rightarrow$  (int  $\rightarrow$  unit)  $\rightarrow$  unit:

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This gives the following strategy:

$$x: \texttt{var} \to f: (\texttt{int} \to \texttt{unit}) \to \texttt{unit}$$

run

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# Changing the type of read

The read operation becomes  $\texttt{let}: \texttt{var} \rightarrow (\texttt{int} \rightarrow \texttt{unit}) \rightarrow \texttt{unit}$ :

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This gives the following strategy:



But we have space to make it more concurrent!

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But we have space to make it more concurrent!

This gives the following strategy:

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Consider  $t = \text{let } x \ (\lambda n.\text{write } y \ 1; n+1)$ :

 $x: \texttt{var} \to y: \texttt{var} \longrightarrow \texttt{int}$ 

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# Conclusion

#### Summary.

- We defined an *denotational* and *extensible* interpretation of concurrent programs in terms of *event structures*.
- The interpretation is parametric over the architecture.

#### Extensions.

- ► We can define sub-models of *&* corresponding to actual architectures.
- The model is inspired from a game semantics model and simplified in this first-order setting.

#### To go further.

- Look at barriers
- Compare that with axiomatic semantics (executions)
- Theorems?