Weak memory models using event structures

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April 3rd, 2016 GaLoP 2016 A simple concurrent and imperative program:

$$\begin{array}{c|c} x, y \text{ initialized to } 0\\ x := 1 & y := 2\\ r \leftarrow y & s \leftarrow x\\ \text{shared variable} \cdot \text{local register} \end{array}$$

Expected outcome: $r \neq 0 \lor s \neq 0$.

A simple concurrent and imperative program:

$$\begin{array}{c|c} x, y \text{ initialized to } 0\\ x &:= 1 \\ r \leftarrow y \\ s \leftarrow x \\ \text{shared variable} \cdot \text{local register} \end{array}$$

Expected outcome: $r \neq 0 \lor s \neq 0$. Wrong on modern architectures (x86, ARM, ...). A simple concurrent and imperative program:

$$\begin{array}{c|c} x, y \text{ initialized to } 0 \\ r \leftarrow y \\ x := 1 \end{array} \begin{vmatrix} s \leftarrow x \\ y := 2 \end{vmatrix}$$
shared variable \cdot local register

Expected outcome: $r \neq 0 \lor s \neq 0$. Wrong on modern architectures (x86, ARM, ...).

Unexpected behaviours

Another simple program:

$$\begin{array}{c|c} x := 1 \\ s \leftarrow x \\ t \leftarrow y \end{array} \middle| \begin{array}{c} y := 1 \\ s' \leftarrow y \\ t' \leftarrow x \end{array}$$

Expected outcome: $s = s' = 1 \Rightarrow t = t' = 1$

Another simple program:

$$\begin{array}{c|c} x & := 1 \\ s & \leftarrow x \\ t & \leftarrow y \end{array} \begin{vmatrix} y & := 1 \\ s' & \leftarrow y \\ t' & \leftarrow x \end{array}$$

Expected outcome: $s = s' = 1 \Rightarrow t = t' = 1$

Wrong even without read exchange (Read Own Write Early).

A need to specify the behaviour

What are the expected behaviour of a concurrent program? \rightarrow It depends on the architecture.

Architectures need to be specified:

- what instructions can be reordered?
- how are writes propagated from one thread to the other?

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What are the expected behaviour of a concurrent program? \rightarrow It depends on the architecture.

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- how are writes propagated from one thread to the other?

To that end, manufacturers provide prosaic documents, but:

- ambiguity: behaviours that are not specified
- inconsistent: some observations may not be predicted.

Some architectures:

- ▶ SC (Sequential consistency): no reordering, sequential memory.
- ARM: reordering of instructions targeting different variables, write caches.

▶ x86: ...

Semantics saves the day

Semantics: Formalize mathematically the vendors specifications:

- get a (possibly computer-verified) proof of non-ambiguity,
- implement the specifications and mechanically test it against real life architectures.

Two main types of semantics among existing models:

- operational semantics: executions are described by runs of an abstract machine,
- axiomatic semantics: the notion of valid execution is axiomatized.

Those models are called *weak memory models*.

This talk

Outline of the talk:

- 1. Reminder on the interpretation of shared memory concurrency in game semantics
- 2. How to change the interpretation of state to accomodate a concrete model: x86-TS0
- 3. Using those ideas to give a concrete model for the first-order fragment dealing with weak memory models.

Our challenge, x86-TS0:

- A read and a write on different memory addresses can be reordered inside a thread.
- A write need not be immediatly committed to main memory. Once it is, it is available to all threads.

I. USUAL MODEL OF IDEALIZED PARALLEL ALGOL

The good ol' IPA

The syntax and semantics of IPA

IPA: Concurrent programming language with shared variables based on the simply-typed λ -calculus.

 $A, B ::= \mathbb{B} \mid \mathbb{N} \mid \mathbf{com} \mid \mathbf{ref} \mid A \rightarrow B$

 $M, N ::= \dots \mathsf{PCF} \text{ constructs...}$ | !M | M := N | M; N| new x in t $| t \parallel u$

Existing games models:

- (Ghica-Murawski) Strategies as sets of non-alternating traces
- ► (C, Clairambault, Winskel) Strategies as event structures

Talk mostly agnostic about the representation.

Interpretation of the state: pure part Intepretation of var as $\mathbb{N} \times \prod_{n \in \mathbb{N}} \text{com}$:

re	wro	\mathtt{wr}_1	
	÷	÷	
n	ok	ok	

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With the following accessors [presented as innocent strategies]:



Interpretation of the state: the cell strategy

To interpret the new construct (the only one to break innocence):

1. Define the set of traces cell as C = 0 with:

$$C(k) ::= \epsilon$$

$$| re \cdot k \cdot C(k) \qquad (Reading from the cell)$$

$$| wr_n \cdot ok \cdot C(n) \qquad (Writing on the cell)$$

A term $x : ref \vdash t : X$ sees x as *volatile* – reading on it can yield any value. Precomposing with cell enforces a particular memory discipline.

Interpretation concurrency:

The strategy $\parallel: \mathbf{com} \to \mathbf{com} \to \mathbf{com}$ is not sequential but is still innocent in a generalized sense.

 \rightarrow We have now a **dag**:



Those dags can be composed inside CHO.

Weakening the model

Problem: can we change the interpretation to match TSO?

Two issues:

- Handling instruction reordering: how to change re and wr to model reorderings?
- Changing the memory discipline: the memory discipline of TSO depends on the notion of threads absent from IPA.

 \rightarrow We need a new language to solve this.

II. IPA/x86: A less idealized programming language

A taste of metal in your IPA.

Syntax of IPA/x86

Reading/write to a reference is modified to handle reorderings:

M, *N* ::= ...PCF constructs...

 $| \operatorname{let}_{\iota} r = !x \text{ in } N | (x :=_{\iota} M; N) \qquad \iota \in \mathbb{N} \text{ is the thread-id}$ $| \operatorname{new} x \text{ in } t | M || N$

There is no sequential composition anymore: operations take directly their continuation:

$$\frac{\Gamma, r: \mathbb{N}, x: \operatorname{ref} \vdash N : \operatorname{com} \quad \Gamma \vdash M : \operatorname{ref}}{\Gamma \vdash \operatorname{let}_{k} r = !x \text{ in } N : \operatorname{com}}$$
$$\frac{\Gamma, x: \operatorname{ref} \vdash M : \operatorname{ref} \quad \Gamma \vdash N : \operatorname{com}}{\Gamma \vdash x :=_{k} M; N}$$

New interpretation of ref:

$$\begin{array}{cccc} \mathbf{r}\mathbf{e}^{\iota} & \mathbf{w}\mathbf{r}_{0}^{\iota} & \mathbf{w}\mathbf{r}_{1}^{\iota} & \dots \\ & & & \\ & & & \\ n & \mathrm{ok} & \mathrm{ok} & \dots \end{array}$$

A dirty trick

How to interpret those new construct? Naive idea:

▶ let_{ι} : ref \rightarrow ($\mathbb{N} \rightarrow$ com) \rightarrow com

•
$$wr_{\iota} : ref \rightarrow \mathbb{N} \rightarrow com \rightarrow com$$

Not enough to **inspect** of the continuation.

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Not enough to inspect of the continuation.

Use instead:

- ▶ let_{ι} : ref → (\mathbb{N} → ref → com) → com
- ▶ $wr_{\iota} : ref \rightarrow \mathbb{N} \rightarrow (ref \rightarrow com) \rightarrow com$

with:

$$[[let_{\iota} r = !x in N]] = let_{\iota} \odot \langle [[x]], \lambda r.\lambda x.[[N]] \rangle$$
$$[[x :=_{\iota} M; N]] = wr_{\iota} \odot \langle [[x]], \lambda x.[[N]] \rangle$$

$$\mathsf{let}_\iota: \quad \mathsf{ref} o (\mathbb{N} \to \mathsf{ref} \to \mathsf{com}) \to \mathsf{com}$$

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run

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Still sequential. Can we use the space to do better?

A concurrent interpretation for let

Idea: start the evaluation of both arguments in parallel.

 $\mathsf{let}_\iota: \quad \mathsf{ref} \to (\mathbb{N} \to \mathsf{ref} \to \mathsf{com}) \to \mathsf{com}$

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$$\mathsf{let}_{\iota}: \quad \mathsf{ref} \to (\mathbb{N} \to \mathsf{ref} \to \mathsf{com}) \to \mathsf{com}$$


$$re^{\iota} \xleftarrow{run} \operatorname{run}^{\mathsf{run}}$$

$$\mathsf{let}_\iota: \quad \mathsf{ref} \to (\mathbb{N} \to \mathsf{ref} \to \mathsf{com}) \to \mathsf{com}$$

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Two synchronizations points:

- One for data dependency
- One to sequentialize operations on x

The strategy for wr is done similarly (without data dependency).

$let_0 r = !x in$ Take x : ref, y : ref $\vdash M = let_0 s = !y in : com$. $y :=_0 r$

 $let_0 r = !x in$ Take x : ref, y : ref $\vdash M = let_0 s = !y in : com$. $y :=_0 r$

$$x : \mathbf{ref} \to y : \mathbf{ref} \to \mathbf{com}$$

run

$$let_0 r = !x in$$

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A strategy cell that represents a TSO memory

Instruction reorderings: check. What about relaxed memory? \rightarrow Update the grammar of valid traces. Now parametrized over:

- a global value n
- *thread-local* local values $\mu : \mathbb{N} \to \mathbb{N} \cup \{\star\}$

$$\begin{split} \mathcal{C}(\mu, n) &::= \epsilon \\ & \mid \mathbf{r} \mathbf{e}^{\iota} \cdot \mu(\iota) \cdot \mathcal{C}(\mu, n) & (\mu(\iota) \neq \star) \\ & (\text{Read from local cache}) \\ & \mid \mathbf{r} \mathbf{e}^{\iota} \cdot n \cdot \mathcal{C}(\mu, n) & (\mu(\iota) = \star) \\ & (\text{Read from the global memory}) \\ & \mid \mathbf{w} \mathbf{r}_{k}^{\iota} \cdot ok \cdot \mathcal{C}(\mu[\iota \leftarrow k], n) \\ & (\text{Write to local cache}) \\ & \mid \mathcal{C}(\mu[\iota \leftarrow \star], \mu(\iota)) & (\mu(\iota) \neq \star) \\ & (\text{Committing a write}) \end{split}$$

This gives a strategy cell_{TSO}.

Remember the program at the beginning:

$$\begin{array}{c|c} x :=_0 1; & y :=_0 1; \\ |et_0 \ s \ = !x \ in \\ |et_0 \ t \ = !y \ in \end{array} \\ |et_0 \ t' \ = !x \ in \end{array}$$

The following is a valid trace of $cell_{TSO}$ (hence can describe a valid interaction on x for instance)

$$wr_1^0 \cdot ok \cdot re^0 \cdot 1 \cdot re^1 \cdot 0$$

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III. THE FIRST-ORDER CASE

Filtering out the higher-order hop

Getting rid of game semantics

► To study the weak memory aspects, the first-order is enough.

→ Simpler presentation of the ideas in the first-order fragment? (terms of the form $x : ref, y : ref \vdash t : com$)

Eliminate game semantics bureaucracy:

- Consider the projection on the left-hand side (sequence of ref)
- We collapse re^t_x · k into one event R^(t,k)
 (Similarly writes are collapsed in W^(t,k)_x)

Overview of the model

- The model is parametrized over an architecture 𝒜 = (→𝔄, 𝔅𝔄) where
 - → A is a relation indicating which instruction ordering cannot be relaxed.
 - $\mathscr{E}_{\mathscr{A}}$ is an event structure describing the memory discipline.

Overview of the model

- ► The model is parametrized over an architecture $\mathscr{A} = (\twoheadrightarrow_{\mathscr{A}}, \mathscr{E}_{\mathscr{A}})$ where
 - → J is a relation indicating which instruction ordering cannot be relaxed.
 - $\mathscr{E}_{\mathscr{A}}$ is an event structure describing the memory discipline.
- The semantics is in two steps:
 - The volatile part: which is the pure functional part (before pre-composition with cell). Defined by a simple *induction* on the program syntax using →A.
 - The closed part: after pre-composition with cell. Defined as the synchronized product with *E_A*.





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Example with \mathcal{E}_{TSO}



(Volatile semantics for SC)
$$\begin{array}{c|c} x :=_{0} 1; \\ |et_{0} \ s = !x \text{ in} \\ |et_{0} \ t = !y \text{ in} () \end{array} \middle| \begin{array}{c} y :=_{0} 1; \\ |et_{0} \ s' = !y \text{ in} \\ |et_{0} \ t' = !x \text{ in} () \end{array}$$



(Computing $\llbracket p \rrbracket_{SC}^O \land \mathscr{E}$)

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$$\begin{array}{c|c} x :=_{0} 1; \\ |e_{t_{0}} s = !x \text{ in} \\ |e_{t_{0}} t = !y \text{ in} () \\ \end{array} \right| \begin{array}{c} y :=_{0} 1; \\ |e_{t_{0}} s' = !y \text{ in} \\ |e_{t_{0}} t' = !x \text{ in} () \\ \end{array}$$



(Computing $\llbracket p \rrbracket_{SC}^O \land \mathscr{E}$)

We can observe $s = s' = 1 \land t = t' = 0$.

Conclusion

Summary.

- We shown a few ideas how to model weaker memory model using game semantics
- We used those ideas to give a parametric denotational semantics for weak memory models, based on event structures.

Perspectives and future work.

- Adding barriers to the mix
- Link with existing semantics (eg. axiomatic semantics)
- Instruction semantics? (modelling a ASM-like language)